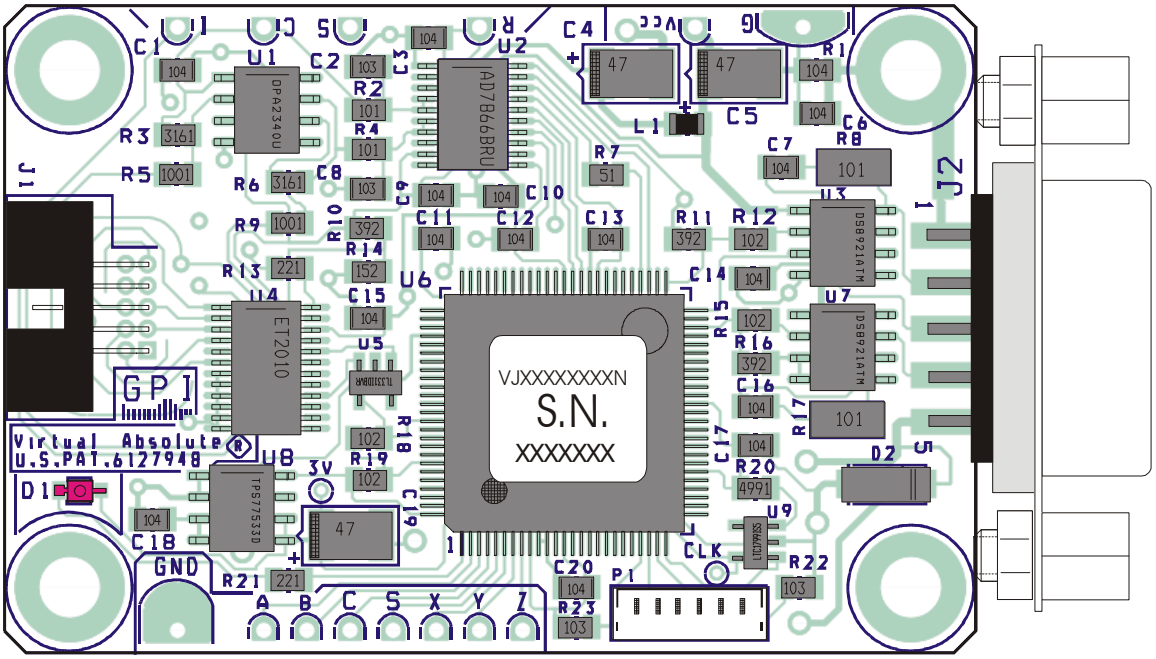
Model VJ

Virtual Absolute™ Interpolating Decoder

USER'S MANUAL

REV 6 JULY 12, 2016



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Overview

The model VJ Interpolating Decoder is designed to be used with the Gurley 7700A02048R12U or 7700A01024R12U read heads. The VJ will decode absolute position from a *Virtual Absolute*™ disk (10 or 11 bits) and interpolate the analog signals to get an additional 8 bits of resolution for a total of 18 or 19 bits. Data is read over a serial RS422 interface. The interface can be used as standard SSI with a single input CLK signal (differential pair) and single output DATA signal (differential pair). There is an optional Sync input (differential pair) that allows for compatibility with other common serial interfaces.

SPECIFICATIONS

POWER: 5.00 VDC @ 150 mA Min = 4.75 VDC, Max = 5.25 VDC

INPUT: 1-2 µA photocurrents from 7700A read head

RESOLUTION:

VJ10 = 262144 measuring steps

VJ11 = 524288 measuring steps

TEMPERATURE RANGE:

Code C = 0 to 70 C

Code A = -40 to 85 C

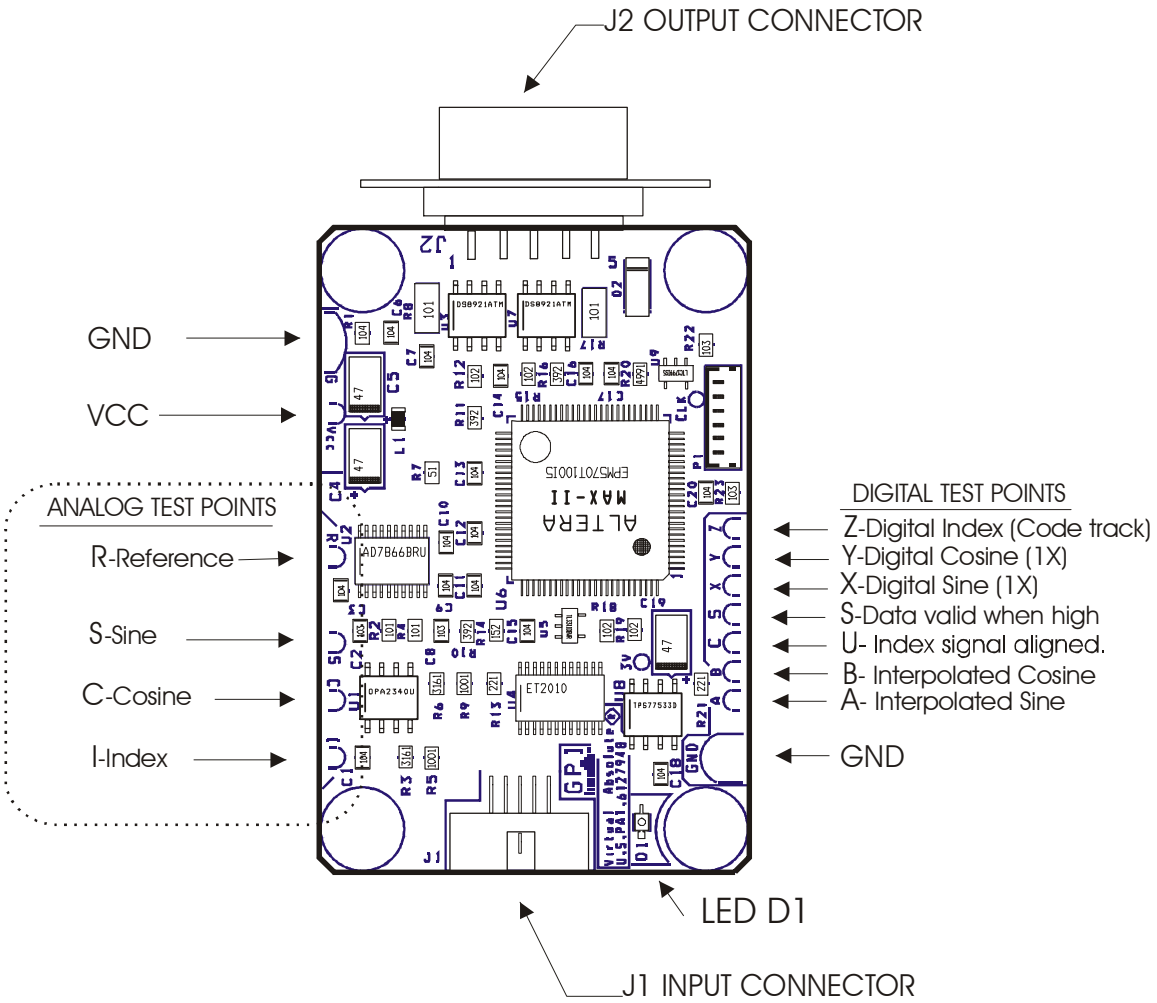
OUTPUT INTERFACE:

CLOCK = RS-422 input

DATA = RS-422 output

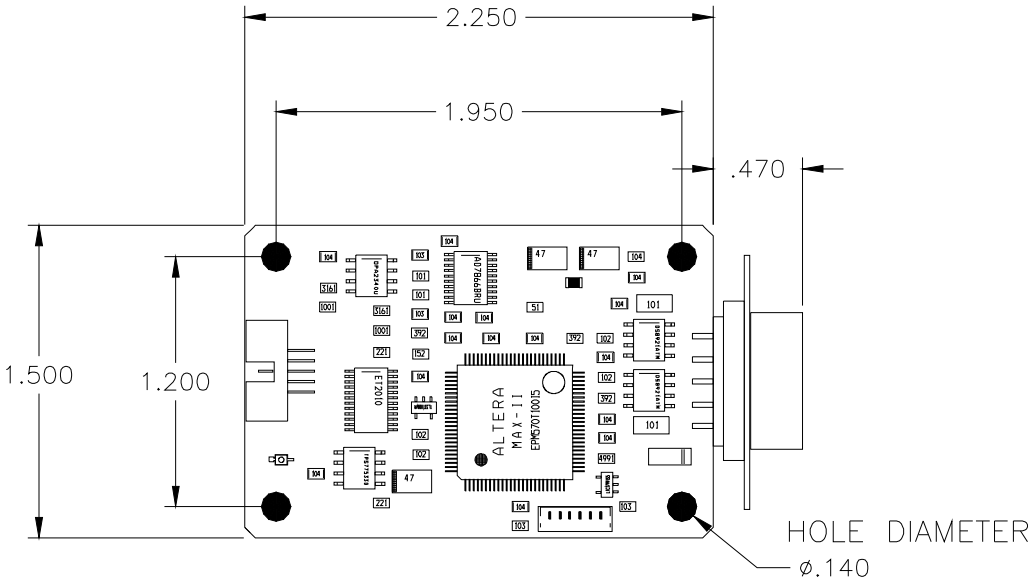
SYNC = RS-422 input (optional)

Figure 1: Board Layout



INSTALLATION

Connect a 7700A readhead to connector J1. Power and RS-422 serial interface is provided by J2. See Figure 2 and Table 1.


2.250
1.950
.470
1.500
1.200
ALTERA
MAX-II
EPM570T100I5
HOLE DIAMETER
ø.140

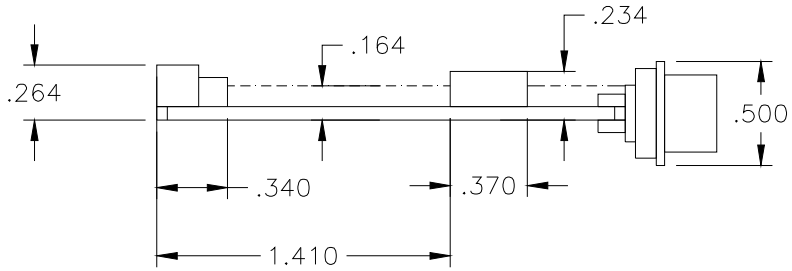

.234
.164
.264
.500
.340
.370
1.410

FIGURE 2: Output connector J2

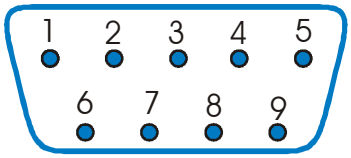
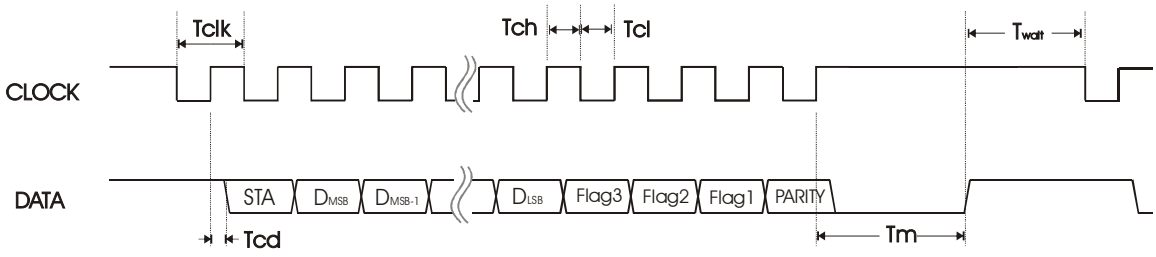


TABLE 1: J2 connector definition

PIN	NAME	DESCRIPTION
1	VCC	5Vdc power input.
2	-SYNC	Optional RS422 input .
3	-CLOCK	RS422 input, SSI clock.
4	+CLOCK	RS422 input, SSI clock
5	CHASSIS	Chassis or shield connection
6	GND	power and signal ground
7	+SYNC	Optional RS422 input .
8	-DATA	RS422 output, SSI Data
9	+DATA	RS422 output, SSI Data

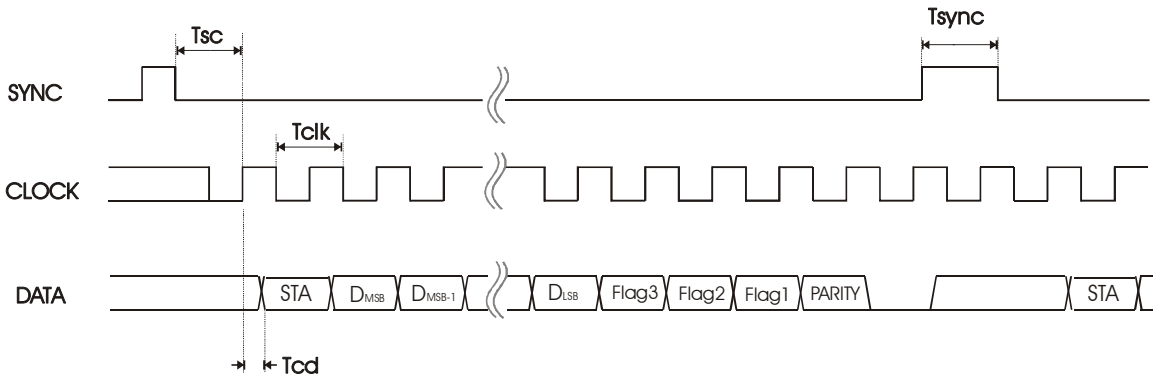
The serial interface timing is shown in figures 2 and 3. Figure 2 shows standard SSI timing. The Sync input can be left disconnected or set to logic 1. (+SYNC voltage greater than -SYNC voltage). Figure 3 shows the timing when using the optional Sync pulse. Data is sampled on the falling edge of SYNC.

FIGURE 2: SSI timing diagram



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
Tclk	Clock period	0.3	1	15	uSec.
Tch	Clock high time	120			nSec.
Tcl	Clock low time	120			nSec.
Tcd	Clock to Data Valid	100		200	nSec.
Tm	Monostabe time	16	20	25	uSec
Twait	Wait Time	0		∞	uSec

FIGURE 3: Timing diagram when using optional SYNC input



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
Tclk	Clock period	0.3	1	∞	uSec.
Tch	Clock high time	120			nSec.
Tcl	Clock low time	120			nSec.
Tcd	Clock to Data Valid	100		200	nSec
Tsync	Sync Pulse width	100		∞	nSec
Tsc	Sync low to CLK rising	100		∞	nSec.

There 7700 read head and disk should be installed according to their manual. It may be necessary to slightly adjust the alignment of the readhead to get the signals in proper phase shown in Figure 5. The Index signal should be at its minimum or maximum level when the cosine signal is at it minimum. The simplest (but not the best way) to make the adjustment is to slightly move readhead until the LED D1 remains lit without blinking, when slowly rotating the disk. A better method is to monitor the voltage on Testpoint U and adjust the read head position until this voltage is at maximum. This pin will be at a high voltage (about 3.3V) when Index transitions occur within +/- 45 degrees of optimum. You can also observe the signals shown in Figure 5 on an oscilloscope while adjusting the head.

FIGURE 4: Read head and disk.

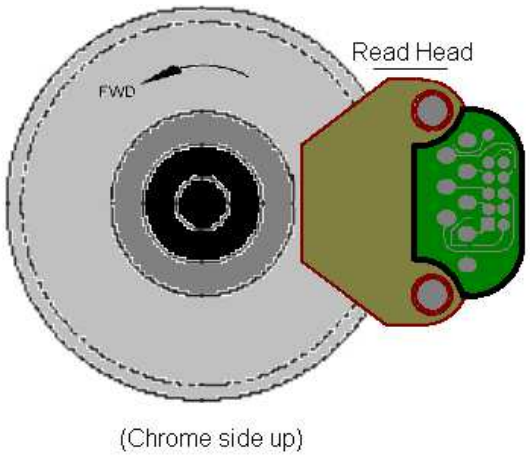
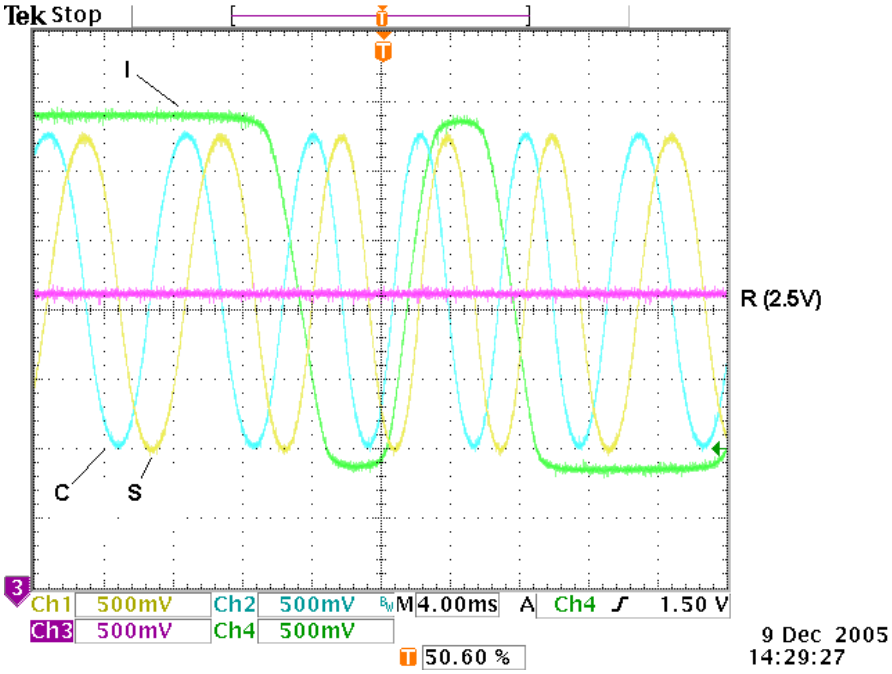


FIGURE 5: Analog test point signals. C,S,I, and R. (Reverse Direction show)



DATA OUTPUT FORMAT

Data is output serially with the first bit being status (STA). The status bit is high when virtual absolute position is not known. After a small initial movement the status bit should go low and stay low. The second bit is the MSB of the position word. Following the LSB of the position word are three flags bits. Flag 1 goes high when a decoding error occurs. Flag 2 goes high when either the analog signal amplitudes become too low (Sin or Cosine < 1Vpp) or the Index signal transitions are occurring in the wrong place. Flag 3 goes high when a quadrature error is detected. This occurs if SIN and COS states change by more than 90 degrees between a sample. A flag bit is set by an error and will be held until a read is completed. The next bit is a parity bit. The parity of all the bits is odd.

TABLE 2: Data format

BIT POSITION	BIT NAME	DESCRIPTION
Bit 1	STA	VA Decoder Status Bit.
Bit 2 thru Bit (n+1)	$D_{MSB}..D_{LSB}$	Position bits.
Bit (n+2)	Flag 3	Quadrature error.
Bit (n+3)	Flag 2	Signal quality watchdog.
Bit (n+4)	Flag 1	VA decoder error.
Bit (n+5)	Parity	Parity bit. Parity is odd.
Bit (n+6)	(0 bit)	Trailing zero bit.

* n is the number of position bits

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2. Make sure your product is properly packed so it is not damaged in shipment.
3. Before you seal the box, write the RMA number on a piece of paper and put it ***inside*** the box so it’s the first thing we see when we open it.
4. Also write the RMA number on the ***outside*** of the box, next to the address label. Use a black felt-tipped marker.
5. If you contact us about the returned item or items, please refer to the appropriate RMA number for quickest service.

Thank you for your cooperation.